

Claims

What is claimed is:

1 1. A semiconductor device comprising:

2 a transmitter, receiver, and transmission line formed within the semiconductor device,
3 wherein the transmitter, receiver, and transmission line are adapted to control data transfer
4 between a first core and a second core within the semiconductor device, wherein the transmitter
5 is adapted to send a signal over the transmission line to the receiver adapted to receive the signal,
6 wherein the receiver is further adapted to create an impedance mismatch to indicate that the
7 second core is unable to transfer the data, and wherein the transmitter is adapted to detect the
8 impedance mismatch.

1 2. The semiconductor device of claim 1, wherein the receiver is further adapted to change an
2 impedance of the transmission line to create the impedance mismatch.

1 3. The semiconductor device of claim 2, wherein the receiver comprises a capacitor adapted to
2 change the impedance of the transmission line.

1 4. The semiconductor device of claim 1, wherein the transmitter is further adapted to terminate
2 the data transfer upon detection of the impedance mismatch.

1 5. The semiconductor device of claim 1, wherein the first core and the second core are each
2 selected from the group consisting of a microcontroller, a microprocessor, and an integrated
3 circuit.

1 6. The semiconductor device of claim 1, wherein the signal is a voltage signal, and wherein the
2 transmitter is adapted to receive a reflection of the voltage signal.

1 7. The semiconductor device of claim 1, wherein the transmitter comprises a voltage comparator
2 adapted to compare an amplitude of the voltage signal to an amplitude of the reflection of the
3 voltage signal.

1 8. The semiconductor device of claim 7, wherein the voltage comparator is further adapted
2 generate a control signal and transmit the control signal to the first core.

1 9. The semiconductor device of claim 8, wherein the control signal is an enable signal adapted to
2 enable the data transfer between the first core and the second core.

1 10. The semiconductor device of claim 8, wherein the control signal is a disable signal adapted
2 to disable the data transfer between the first core and the second core.

- 1 11. A method for controlling data transfer, comprising:
2 providing a transmitter, a receiver, and a transmission line for controlling the data
3 transfer between a first core and a second core within a semiconductor device;
4 sending, by the transmitter, a signal over the transmission line to the receiver;
5 creating, by the receiver, an impedance mismatch to indicate that the second core is
6 unable to transfer the data between the first core and the second core; and
7 detecting, by the transmitter, the impedance mismatch.
- 1 12. The method of claim 11, further comprising creating the impedance mismatch by changing
2 an impedance of the transmission line.
- 1 13. The method of claim 11, further comprising using a capacitor in the receiver to change the
2 impedance of the transmission line.
- 1 14. The method of claim 11, further comprising terminating by the transmitter, the data transfer
2 upon detection of the impedance mismatch.
- 1 15. The method of claim 11, wherein the signal is a voltage signal; and
2 receiving by the transmitter, a reflection of the voltage signal.
- 1 16. The method of claim 15, wherein the transmitter comprises a voltage comparator; and

2 comparing by the voltage comparator, an amplitude of the voltage signal to an amplitude
3 of the reflection of the voltage signal.

1 17. The method of claim 16, further comprising:

2 generating by the voltage comparator, a control signal; and
3 transmitting by the voltage comparator the control signal to the first core.

1 18. The method of claim 17, wherein the control signal is a disable signal, and further

2 comprising

3 disabling by the disable signal, the data transfer between the first core and the second
4 core.

1 19. The method of claim 11, further comprising:

2 creating by the receiver, an impedance match to indicate that the second core is able to
3 transfer the data between the first core and the second core; and
4 detecting by the transmitter, the impedance match.

1 20. The method of claim 11, wherein the first core and the second core are selected from the
2 group consisting of a microcontroller, a microprocessor, and an integrated circuit.